DESCRIPTION
The NE572 is a dual-channel, high-performance gain control circuit in which either channel may be used for dynamic range compression or expansion. Each channel has a full-wave rectifier to detect the average value of input signal, a linearized, temperature-compensated variable gain cell ($\Delta G$) and a dynamic time constant buffer. The buffer permits independent control of dynamic attack and recovery time with minimum external components and improved low frequency gain control ripple distortion over previous compandors.

The NE572 is intended for noise reduction in high-performance audio systems. It can also be used in a wide range of communication systems and video recording applications.

FEATURES
- Independent control of attack and recovery time
- Improved low frequency gain control ripple
- Complementary gain compression and expansion with external op amp
- Wide dynamic range—greater than 110dB
- Temperature-compensated gain control
- Low distortion gain cell
- Low noise—6µV typical
- Wide supply voltage range—6V-22V
- System level adjustable with external components

APPLICATIONS
- Dynamic noise reduction system
- Voltage control amplifier
- Stereo expander
- Automatic level control
- High-level limiter
- Low-level noise gate
- State variable filter

ORDERING INFORMATION

<table>
<thead>
<tr>
<th>DESCRIPTION</th>
<th>TEMPERATURE RANGE</th>
<th>ORDER CODE</th>
<th>DWG #</th>
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<tbody>
<tr>
<td>16-Pin Plastic Small Outline (SO)</td>
<td>0 to +70°C</td>
<td>NE572D</td>
<td>0005</td>
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<tr>
<td>16-Pin Plastic Dual In-Line Package (DIP)</td>
<td>0 to +70°C</td>
<td>NE572N</td>
<td>0406</td>
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<tr>
<td>16-Pin Plastic Small Outline (SO)</td>
<td>–40 to +85°C</td>
<td>SA572D</td>
<td>0005</td>
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<td>16-Pin Ceramic Dual In-Line Package (Cerdip)</td>
<td>–40 to +85°C</td>
<td>SA572F</td>
<td>0582</td>
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<td>16-Pin Plastic Dual In-Line Package (DIP)</td>
<td>–40 to +85°C</td>
<td>SA572N</td>
<td>0406</td>
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ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>RATING</th>
<th>UNIT</th>
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</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>Supply voltage</td>
<td>22</td>
<td>$V_{DC}$</td>
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<tr>
<td>$T_A$</td>
<td>Operating temperature range</td>
<td>NE572</td>
<td>0 to +70</td>
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<td></td>
<td></td>
<td>SA572</td>
<td>–40 to +85</td>
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<tr>
<td>$P_D$</td>
<td>Power dissipation</td>
<td>500</td>
<td>mW</td>
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Programmable analog compandor

NE/SA572

DC ELECTRICAL CHARACTERISTICS

Standard test conditions (unless otherwise noted) $V_{CC}=15V$, $T_A=25°C$; Expander mode (see Test Circuit). Input signals at unity gain level (0dB) = 100m$V_{RMS}$ at 1kHz; $V_1 = V_2$; $R_2 = 3.3kΩ$; $R_3 = 17.3kΩ$.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>NE572</th>
<th>SA572</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
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<td>$V_{CC}$</td>
<td>Supply voltage</td>
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<td>6</td>
<td>22</td>
<td>6</td>
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<tr>
<td>$I_{CC}$</td>
<td>Supply current</td>
<td>No signal</td>
<td>6</td>
<td></td>
<td>6.3</td>
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<td>$V_R$</td>
<td>Internal voltage reference</td>
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<td>2.5</td>
<td>2.7</td>
<td>2.3</td>
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<td>THD</td>
<td>Total harmonic distortion (untrimmed)</td>
<td>$1kHz C_A=1.0μF$</td>
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<td>1.0</td>
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<td>THD</td>
<td>Total harmonic distortion (trimmed)</td>
<td>$1kHz C_R=10μF$</td>
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<td>THD</td>
<td>Total harmonic distortion (trimmed)</td>
<td>$100Hz$</td>
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<td>No signal output noise</td>
<td>Input to $V_1$ and $V_2$ grounded (20–20kHz)</td>
<td>6</td>
<td>25</td>
<td>6</td>
<td>25</td>
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<td>DC level shift (untrimmed)</td>
<td>Input change from no signal to $100mV_{RMS}$</td>
<td>±20</td>
<td>±50</td>
<td>±20</td>
<td>±50</td>
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<td>Unity gain level</td>
<td>$V_1=V_2=400mV$</td>
<td>−1</td>
<td>0</td>
<td>+1</td>
<td>−1.5</td>
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<td>Large–signal distortion</td>
<td>Rectifier input</td>
<td>$V_2=+6dB V_1=0dB$</td>
<td>±0.2</td>
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<td>±0.2</td>
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<td></td>
<td>Rectifier input</td>
<td>$V_2=-30dB V_1=0dB$</td>
<td>±0.5</td>
<td>−1.5</td>
<td>±0.5</td>
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<td></td>
<td>Rectifier input</td>
<td>$V_2=-2dB V_1=0dB$</td>
<td>±0.8</td>
<td>+1.6</td>
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<td>Channel crosstalk</td>
<td>200m$V_{RMS}$ into channel A, measured output on channel B</td>
<td>60</td>
<td></td>
<td>60</td>
<td></td>
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<td>PSRR</td>
<td>Power supply rejection ratio</td>
<td>120Hz</td>
<td>70</td>
<td>70</td>
<td>$dB$</td>
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Programmable analog compandor

NE/SA572

October 7, 1987

4

TEST CIRCUIT

AUDIO SIGNAL PROCESSING IC COMBINES VCA AND FAST ATTACK/SLOW RECOVERY LEVEL SENSOR

In high-performance audio gain control applications, it is desirable to independently control the attack and recovery time of the gain control signal. This is true, for example, in compandor applications for noise reduction. In high end systems the input signal is usually split into two or more frequency bands to optimize the dynamic behavior for each band. This reduces low frequency distortion due to control signal ripple, phase distortion, high frequency channel overload and noise modulation. Because of the expense in hardware, multiple band signal processing up to now was limited to professional audio applications.

With the introduction of the Signetics NE572 this high-performance noise reduction concept becomes feasible for consumer hi fi applications. The NE572 is a dual channel gain control IC. Each channel has a linearized, temperature-compensated gain cell and an improved level sensor. In conjunction with an external low noise op amp for current-to-voltage conversion, the VCA features low distortion, low noise and wide dynamic range. The NE572 is assembled in a standard 16-pin dual in-line plastic package and in oversized SOL package. It operates over a wide supply range from 6V to 22V. Supply current is less than 6mA. The NE572 is designed for consumer application over a temperature range 0-70 °C. The SA572 is intended for applications from –40 °C to +85 °C.

NE572 BASIC APPLICATIONS

Description

The NE572 consists of two linearized, temperature-compensated gain cells (ΔG), each with a full-wave rectifier and a buffer amplifier as shown in the block diagram. The two channels share a 2.5V common bias reference derived from the power supply but otherwise operate independently. Because of inherent low distortion, low noise and the capability to linearize large signals, a wide dynamic range can be obtained. The buffer amplifiers are provided to permit control of attack time and recovery time independent of each other. Partitioned as shown in the block diagram, the IC allows flexibility in the design of system levels that optimize DC shift, ripple distortion, tracking accuracy and noise floor for a wide range of application requirements.

Gain Cell

Figure 1 shows the circuit configuration of the gain cell. Bases of the differential pairs Q1-Q2 and Q3-Q4 are both tied to the output and inputs of OPA A1. The negative feedback through Q1 holds the VBE of Q1-Q2 and the VBE of Q3-Q4 equal. The NE572 is designed for consumer application over a temperature range 0-70 °C. The SA572 is intended for applications from –40 °C to +85 °C.

\[ \Delta V_{BE_{Q1Q2}} = \Delta V_{BE_{Q3Q4}} \]

\( V_{BE} = V_T I_{IN} IC/IS \)
Programmable analog compandor  NE/SA572

where \( I_{IN} = \frac{V_{IN}}{R_1} \)
\[
R_1 = 6.8k\Omega
I_1 = 140\mu A
I_2 = 280\mu A
\]

\[
I_O = \frac{1}{2} \frac{I_G}{I_S} \frac{1}{2} \frac{I_O}{I_S}
\]
(2)

\[
V_{TH} \frac{1}{2} \frac{I_G}{I_S} \frac{1}{2} \frac{I_O}{I_S}
\]

\[
V_{TH} \frac{1}{2} \frac{I_G}{I_S} \frac{1}{2} \frac{I_O}{I_S}
\]

\( I_O \) is the differential output current of the gain cell and \( I_G \) is the gain control current of the gain cell.

If all transistors Q1 through Q4 are of the same size, equation (2) can be simplified to:

\[
I_O = \frac{2}{I_2} I_{IN} I_G \frac{1}{I_2} I_2 2I_1 I_G
\]
(3)

The first term of Equation 3 shows the multiplier relationship of a linearized two quadrant transconductance amplifier. The second term is the gain control feedthrough due to the mismatch of devices. In the design, this has been minimized by large matched devices and careful layout. Offset voltage is caused by the device mismatch and it leads to even harmonic distortion. The offset voltage can be trimmed out by feeding a current source within \( \pm 25\mu A \) into the THD trim pin.

The residual distortion is third harmonic distortion and is caused by gain control ripple. In a compandor system, available control of fast attack and slow recovery improve ripple distortion significantly. At the unity gain level of 100mV, the gain cell gives THD (total harmonic distortion) of 0.17% typ. Output noise with no input signals is only 6\mu V in the audio spectrum (10Hz-20kHz). The output current \( I_O \) must feed the virtual ground input of an operational amplifier with a resistor from output to inverting input. The non-inverting input of the operational amplifier has to be biased at V_{REF} if the output current \( I_O \) is DC coupled.

Rectifier

The rectifier is a full-wave design as shown in Figure 2. The input voltage is converted to current through the input resistor \( R_2 \) and turns on either Q5 or Q6 depending on the signal polarity. Deadband of the voltage to current converter is reduced by the loop gain of the gain block A2. If AC coupling is used, the rectifier error comes only from input bias current of gain block A2. The input bias current is typically about 70nA. Frequency response of the gain block A2 also causes second-order error at high frequency. The collector current of Q6 is mirrored and summed at the collector of Q5 to form the full wave rectified output current \( I_R \). The rectifier transfer function is

\[
I_R = \frac{V_{IN}}{R_2}
\]

If \( V_{IN} \) is AC-coupled, then the equation will be reduced to:

\[
I_{RAC} = \frac{V_{IN}(AVG)}{R_2}
\]

The internal bias scheme limits the maximum output current \( I_R \) to be around 300\mu A. Within a \( \pm 1dB \) error band the input range of the rectifier is about 52dB.
Figure 2. Simplified Rectifier Schematic

Figure 3. Buffer Amplifier Schematic

Buffer Amplifier
In audio systems, it is desirable to have fast attack time and slow recovery time for a tone burst input. The fast attack time reduces transient channel overload but also causes low-frequency ripple distortion. The low-frequency ripple distortion can be improved with the slow recovery time. If different attack times are implemented in corresponding frequency spectrums in a split band audio system, high quality performance can be achieved. The buffer amplifier is designed to make this feature available with minimum external components. Referring to Figure 3, the rectifier output current is mirrored into the input and output of the unipolar buffer amplifier A3 through Q8, Q9 and Q10. Diodes D11 and D12 improve tracking accuracy and provide common-mode bias for A3. For a positive-going input signal, the buffer amplifier acts like a voltage-follower. Therefore, the output impedance of A3 makes the contribution of capacitor CR to attack time insignificant. Neglecting diode impedance, the gain Ga(t) for ΔG can be expressed as follows:

\[ Ga(t) = \frac{(Ga_{INT} - Ga_{RNL}) e^{-t/\tau_A}}{Ga_{RNL}} \]

where \( \tau_A \) is the attack time constant and \( R_A \) is a 10k internal resistor. Diode D15 opens the feedback loop of A3 for a negative-going signal if the value of capacitor CR is larger than capacitor CA. The recovery time depends only on CR • RR. If the diode impedance is assumed negligible, the dynamic gain GR(t) for ΔG is expressed as follows.

\[ GR(t) = \frac{(GR_{INT} - GR_{RNL}) e^{-t/\tau_R}}{GR_{RNL}} \]

where \( \tau_R \) is the recovery time constant and RR is a 10k internal resistor. The gain control current is mirrored to the gain cell through Q14. The low level gain errors due to input bias current of A2 and A3 can be trimmed through the tracking trim pin into A3 with a current source of ±3μA.

Basic Expander
Figure 4 shows an application of the circuit as a simple expander. The gain expression of the system is given by
Both the resistors $R_1$ and $R_2$ are tied to internal summing nodes. $R_1$ is a 6.8k internal resistor. The maximum input current into the gain cell can be as large as 140µA. This corresponds to a voltage level of 140µA • 6.8k=952mV peak. The input peak current into the rectifier is limited to 300µA by the internal bias system. Note that the value of $R_1$ can be increased to accommodate higher input level. $R_2$ and $R_3$ are external resistors. It is easy to adjust the ratio of $R_2/R_2$ for desirable system voltage and current levels. A small $R_2$ results in higher gain control current and smaller static and dynamic tracking error. However, an impedance buffer $A_1$ may be necessary if the input is voltage drive with large source impedance.

The gain cell output current feeds the summing node of the external OPA $A_2$. $R_3$ and $A_2$ convert the gain cell output current to the output voltage. In high-performance applications, $A_2$ has to be low-noise, high-speed and wide band so that the high-performance output of the gain cell will not be degraded. The non-inverting input of $A_2$ can be biased at the low noise internal reference Pin 6 or 10. Resistor $R_4$ is used to bias up the output DC level of $A_2$ for maximum swing. The output DC level of $A_2$ is given by

$$V_{ODC} = V_{REF} \frac{R_3}{R_4} \frac{V_B}{R_4}$$

$V_B$ can be tied to a regulated power supply for a dual supply system and be grounded for a single supply system. $CA$ sets the attack time constant and $CR$ sets the recovery time constant. *5COL

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**Figure 4. Basic Expander Schematic**
**Basic Compressor**

Figure 5 shows the hook-up of the circuit as a compressor. The IC is put in the feedback loop of the OPA A1. The system gain expression is as follows:

\[
\frac{V_{OUT}}{V_{IN}} = \frac{I_1}{2} R_2 R_1 \frac{1}{R_3 V_{IN(AVG)}}
\]  

(7)

R\(_{DC1}\), R\(_{DC2}\), and CDC form a DC feedback for A\(_1\). The output DC level of A\(_1\) is given by

\[
V_{ODC} = V_{REF} \left( \frac{R_{DC1}}{R_4} \right) \frac{R_{DC2}}{R_4}
\]  

(8)

The zener diodes D\(_1\) and D\(_2\) are used for channel overload protection.

**Basic Compressor System**

The above basic compressor and expander can be applied to systems such as tape/disc noise reduction, digital audio, bucket brigade delay lines. Additional system design techniques such as bandlimiting, band splitting, pre-emphasis, de-emphasis and equalization are easy to incorporate. The IC is a versatile functional block to achieve a high performance audio system. Figure 6 shows the system level diagram for reference.

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**Figure 5. Basic Compressor Schematic**
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Figure 6. NE572 System Level